## Remarks

For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated July 7, 2008 lists that following objection and rejections: an objection to claim 12; claims 1-9 and 12 stand rejected under 35 U.S.C. § 103(a) over Krakauer *et al.* (US Patent No. 5,617,283) in view of Avery *et al.* (US Patent No. 6,501,632); claim 10 stands rejected under 35 U.S.C. § 103(a) over Krakauer in view of Avery and further in view of Ker *et al.* (US Patent Pub. 2002/0050615); claims 11 and 15 stand rejected under 35 U.S.C. § 103(a) over Krakauer in view of Avery and further in view of Lai *et al.* (US Patent Pub. 2003/0235022); and claims 1-3 and 11-15 stand rejected under 35 U.S.C. § 103(a) over John *et al.* (US Patent No. 6,522,511) in view of Avery.

Regarding the objection to claim 12, Applicant has amended claim 12 to refer to the clamping device. Thus, Applicant requests that the objection to claim 12 be removed.

Applicant respectfully traverses the § 103(a) rejections of claims 1-12 and 15, each of which relies upon a combination of Avery with Krakauer, and the § 103(a) rejections of claims 1-3 and 11-15, each of which relies upon a combination of Avery with John, because none of the cited references teaches or suggests a time-delay circuit including a resistor and a capacitive device connected in series between a power supply and the control inputs of the first and second transistors. The Office Action acknowledges that neither the Krakauer reference nor the John reference teaches a time-delay circuit connected as in the claimed invention. The Office Action then erroneously asserts that Avery teaches that resister $R_{Z1}$ and capacitor C are connected in series between pad 302[1] and the control input of the NMOS transistor. *See, e.g.,* Figure 3. In actuality, Avery teaches that resister $R_{Z1}$ is the internal (or parasitic) resistance of Zener diode Z1, and Avery further teaches that an alternative to using Zener diode Z1 is to use capacitor C (shown in phantom in Figure 3) in lieu of the diode Z1. *See, e.g.,* Col. 3:5-6 and Col. 3:56-61. Thus, Avery teaches that either Zener diode Z1 (*i.e.,* resister $R_{Z1}$) or capacitor C is connected between pad 302 and the

[1] The Office Action cites to pad 301; however, there is no pad 301 in Avery's Figure 3. Thus, Applicant assumes that the Office Action intended to refer to pad 302. If Applicant's assumption is incorrect, Applicant requests clarification and an opportunity to respond thereto prior to a final rejection. See, e.g., M.P.E.P § 706.07.

Zener diode Z1 (*i.e.*, resister $R_{Z1}$) or capacitor C is connected between pad 302 and the control input of the NMOS transistor, not both. As such, the cited portions of Avery do not teach or suggest a time-delay circuit as in the claimed invention.

Moreover, the cited portions of Avery do not teach that Zener diode Z1 (*i.e.*, resister $R_{Z1}$) or capacitor C is connected between the power supply and the control inputs of two transistors (*i.e.*, the first and second transistors) as in the claimed invention. Instead, Avery teaches that Zener diode Z1 or capacitor C is connected between pad 302 and the control input of only a single transistor (*i.e.*, the NMOS transistor). *See, e.g.,* Figure 3. Thus, the Office Action fails to cite to any reference that teaches or suggests a time-delay circuit connected between a power supply and the control inputs of the first and second transistors as in the claimed invention. As such, Applicant submits that any combination that includes such aspects would appear to be based on improper hindsight reconstruction using Applicant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142.

In view of the above, the § 103(a) rejections of all of the claims fail to establish *prima facie* obviousness, based upon the lack of teaching or suggestion of all limitations. Thus, the cited combinations do not correspond to the claimed invention. Accordingly, the § 103(a) rejections of claims 1-12 and 15 based on Krakauer and the § 103(a) rejections of claims 1-3 and 11-15 based on John are improper and Applicant requests that they be withdrawn.

Applicant further traverses all of the § 103(a) rejections because the Office Action fails to provided sufficient detail regarding the proposed combinations to enable Applicant to determine the propriety of such combinations. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply."). The following specific examples identify why the detail provided by the office Action in regards to the proposed combinations is insufficient.

As a first example, regarding the combination of Avery with Krakauer, the Office Action asserts that Krakauer teaches a time-delay circuit that includes transistors 42 and 46 (*see, e.g.,* Figure 2); the Office Action then proposes to modify the circuit of Krakauer to be connected as taught by Avery in regard to resister $R_{Z1}$, capacitor C and Zener diode Z2 (*see, e.g.,* Figure 3). *See, e.g.,* page 5:4-16 of the instant Office Action. The Office Action, however, does not specify how Krakauer's circuit is to be modified (*e.g.,* by connecting transistors 42 and 46 in series between pad 12 and the input of inverter 45, or by replacing transistors 42 and 46 with elements taught by Avery, or in some other undisclosed manner). Thus, should any rejection based on a combination of Avery with Krakauer be maintained, Applicant requests clarification regarding how Krakauer's circuit is being modified. Applicant should also be afforded an opportunity to respond to such clarification prior to a final rejection. *See, e.g.,* M.P.E.P. § 706.07 ("Before final rejection is in order a clear issue should be developed between the examiner and applicant."). In this instance, Applicant submits that a clear issue has not been developed due to the lack of specificity regarding the proposed modification of Krakauer's circuit.

As a second example, regarding the combination of Avery with John, the Office Action asserts that John teaches a time-delay circuit that includes the resister and transistor elements of detector 30 (*see, e.g.,* Figure 3); the Office Action then proposes to modify the circuit of John to be connected as taught by Avery in regard to resister $R_{Z1}$, capacitor C and Zener diode Z2 (*see, e.g.,* Figure 3). *See, e.g.,* page 8:6-22 of the instant Office Action. The Office Action, however, does not specify how John's circuit is to be modified (*e.g.,* by connecting the resister and transistor elements of detector 30 in series between node 18 and the input of inverter 32, or by replacing the resister and transistor elements of detector 30 with elements taught by Avery, or in some other undisclosed manner). Thus, should any rejection based on a combination of Avery with John be maintained, Applicant requests clarification regarding how John's circuit is being modified, to which Applicant should be afforded an opportunity to respond prior to a final rejection as discussed above.

In view of the above, the Office Action fails to provide adequate detail regarding the proposed combinations to enable Applicant to determine the propriety of such combinations. Accordingly, all of the § 103(a) rejections are improper and Applicant requests that they be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 4 because the cited portions of Krakauer do not teach that transistor 46a (*i.e.,* the Office Action's alleged third transistor) is connected between a supply voltage terminal and the control inputs of transistors 45a and 45b (*i.e.,* the Office Action's alleged first and second transistors). Claim 4 requires that the third transistor be connected between the supply voltage terminal and the control inputs of the first and second transistors. Instead, the cited portions of Krakauer teach that transistor 46a is connected between the input of inverter 45 and Vss (*i.e.,* the Office Action's alleged reference voltage terminal). Accordingly, the § 103(a) rejection of claim 4 is improper and Applicant requests that it be withdrawn.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

*Please direct all correspondence to:*

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Robert J. Crawford
Reg. No.: 32,122
(NXPS.446PA)